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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,030	05/15/2001	Tetsuro Asano	492322001000	7974

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EXAMINER

BEHULU, ALEMAYEHU

ART UNIT PAPER NUMBER

2682

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/855,030

Applicant(s)

ASANO ET AL.

Examiner

Alemayehu Behulu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 9 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6</u> . | 6) <input type="checkbox"/> Other: ____ |

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Kim (5, 081, 706).

Regarding claim 1, the prior art discloses a compound semiconductor switching device (figure 6) comprising: a first FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said first FET (figure 6B, left side of the figure, label FET 1, Ctl-1, R1); a second FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said second FET (figure 6 B, right side of the figure, label FET 2, Ctl-2, R2); a common input terminal (figure 6 B, label IN), said common input terminal being formed by connecting one of the signal electrodes of the first FET and one of the signal electrodes of the second FET (figure 6 B, see the two braches of label IN); a first output terminal, said first output terminal being the signal electrode of the first FET not used as the common input terminal (figure 6 B, label OUT1, page 5, lines 4-9); and a second output terminal, said second output terminal being the signal electrode of the second FET not used as the common input terminal (figure 6, label OUT2, page 5, lines 4-9); wherein the gate electrodes of the first and second FET's are provided with control signals such that only one FET allows conduction of electric current so that a signal pass is formed between the common input terminal and either the first output terminal or the

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second output terminal (figure 6 B, label Ctl-1 and Ctl-2, page 2 lines 1-14). However, prior art fails to disclose wherein the first FET and the second FET have gate widths of about 700. μm or less. But, Kim discloses the first FET and the second FET have gate widths of about 700 μm or less (figure 2, column 3, lines 28-40, figure 5, number 42 and 44). Therefore at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine prior art with Kim (5, 081, 706) so that the total semiconductor chip area occupied is decreased as suggested by Kim.

Regarding claim 2, the combination of prior art and Kim disclose a compound semiconductor switching device according to claim 1, wherein an input signal of about 2.4 GHz or higher is applied to the common input terminal, and the first FET and the second FET have gate widths of about 600 μm or less (see Kim column 2, lines 54-68, figure 2, figure 5, number 42 and 44).

Regarding claim 3, the combination of prior art and Kim disclose a compound semiconductor switching device according to claim 1, further comprising a GaAs substrate is used as a semi-insulating substrate for forming the channel layer on a surface thereof (see prior art figure 6A, numbers 1 and 2 and page 1, lines 21-29, page3 lines 1-9).

Regarding claim 4, the combination of prior art and Kim disclose a compound semiconductor switching device according to claim 1, wherein the gate electrode and the channel layer of the first FET and the second FET form Schottky contact, and wherein the signal electrodes and the

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channel layer of the first FET and the second FET form ohmic contacts (see prior art page 1, lines 21-29).

Regarding claim 5, the combination of prior art and Kim disclose a compound semiconductor switching device according to claim 1, wherein the signal electrodes of the first FET are a source electrode and a drain electrode of the first FET, and the signal electrodes of the second FET are a source electrode and a drain electrode of the second FET (see prior art page 1, lines 21-29, page 2, lines 1-14, page 4, lines 4-9).

Regarding claim 6, the combination of prior art and Kim disclose a compound semiconductor switching device according to claim 1, wherein the input signal of about 2.4 GHz or higher is applied to the common input terminal, and the gates widths of the first FET and the second FET are about 600 .mu.m or less (see Kim column 2, lines 54-68, figure 2, figure 5, number 42 and 44); wherein a GaAs substrate is used as a semi-insulating substrate for forming the channel layer on a surface thereof (see prior art figure 6A, numbers 1 and 2 and page 1, lines 21-29, page 3 lines 1-9); and wherein the signal electrodes of the first FET are a source electrode and a drain electrode of the first FET, and the signal electrodes of the second FET are a source electrode and a drain electrode of the second FET (see prior art page 1, lines 21-29, page 2, lines 1-14, page 4, lines 4-9).

2. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Nakao (6, 281, 762).

Regarding claim 7, prior art discloses mobile communication device, comprising: at least one compound semiconductor switching Device (figures 6A and 6B), said compound semiconductor switching devices comprising a first FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said first FET (figure 6B, left side of the figure, label FET 1, Ctl-1, R1); a second FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said second FET (figure 6 B, right side of the figure, label FET 2, Ctl-2, R2); a common input terminal (figure 6 B, label IN), said common input terminal being formed by connecting one of the signal electrodes of the first FET and one of the signal electrodes of the second FET (figure 6 B, see the two braches of label IN); a first output terminal, said first output terminal being the signal electrode of the first FET not used as the common input terminal (figure 6 B, label OUT1, page 4 lines 4-9); and a second output terminal, said second output terminal being the signal electrode of the second FET not used as the common input terminal (figure 6, label OUT2, page 4 lines 4-9); wherein the gate electrodes of the first and second FET's are provided with control signals such that only one FET allows conduction of electric current so that a signal pass is formed between the common input terminal and either the first output terminal or the second output terminal (figure 6 B, label Ctl-1 and Ctl-2, page 2 lines 1-14). However, prior art fails to disclose an antenna for receiving and sending an electromagnetic signal; a signal receiving circuit for receiving the signal through the antenna; a signal transmitting circuit for sending the signal through the antenna; and nd the first FET and the second FET having gate widths of about 700 .mu.m or less; wherein the compound

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semiconductor devices are configured within the mobile communication device for switching between the signal receiving circuit and the signal transmitting circuit. But, Nakao disclose an antenna for receiving and sending an electromagnetic signal; a signal receiving circuit for receiving the signal through the antenna (figure 10, number 41, 42); a signal transmitting circuit for sending the signal through the antenna (figure 10, number 41, 43); and the first FET and the second FET having gate widths of about 700 μm or less (column 6, lines 42-60); wherein the compound semiconductor devices are configured within the mobile communication device for switching between the signal receiving circuit and the signal transmitting circuit (column 1, lines 8-14). Therefore at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine prior art with Nakao (6, 281, 762) so that reductions in the power consumption and transmission loss of the mobile communication apparatus is achieved as suggested by Nakao.

Regarding claim 9, the combination of prior art and Nakao disclose a mobile communication device according to claim 7, further comprising specialized circuitry for a mobile telephone, a Bluetooth device or a wireless LAN (see Nakao column 1, lines 8-14).

Allowable Subject Matter

3. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 8, the applied references fail to disclose, or render obvious the claimed limitations that second antenna, an antenna switch comprising one of said compound semiconductor switching devices for changing between the antenna and the second antenna for better reception or transmission of the signal, a filter switch comprising one of said compound semiconductor switching devices for changing between a filter for receiving the signal or for transmitting the signal and a band switch comprising one of said compound semiconductor switching devices for changing an IF band for receiving the signal or for transmitting the signal as specified in the claim.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vaisanen et al. (U.S. Patent No. 6, 560, 443) Antenna Sharing Switching Circuitry For Multi-Transceiver Mobile Terminal and Method Therefor

Dean et al. (U.S. Patent No. 5, 881, 369) Dual Mode Transceiver

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alemayehu Behulu whose telephone number is 703-305-4828. The examiner can normally be reached on 8 AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AB

Nguyen Vo
4-29-04

**NGUYENT.VO
PRIMARY EXAMINER**